CLAIMS

What is claimed is:

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1. A processor comprising:

a first instruction set engine;

a second instruction set engine;

a mode identifier;

a plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine; and

a floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output.

2. The processor of Claim 1 wherein the mode identifier is one of a plurality of bits in a processor status register.

3. The processor of Claim 1 wherein the floating-point unit comprises:

pre-processing hardware to detect if a token exists in the input;

an arithmetic unit responsive to the input and the mode identifier; and

post-processing hardware to perform a token specific operation if a token exists in the input.

4. The processor of Claim 1 wherein the input includes data stored in at least one of the floating-point registers.

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5. The processor of Claim 1 wherein the input may contain a token, wherein the floating-point registers are 82 bits wide, and wherein the token being an 82 bit processor known value.

6. The processor of Claim 3 wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request

7. The processor of Claim 1 wherein the floating point registers each comprise:

a sign bit,

an exponent; and

a significand.

8. The processor of Claim 1 wherein the mode identifier indicates whether the processor is in a first mode or a second mode.

9. The processor of Claim 1 wherein the mode identifier indicates whether the processor is in a 32 bit word instruction set architecture mode (ISA) or a 64 bit word ISA mode.

10. A method in a processor comprising:

fetching an input from at least one of a plurality of floating-point registers;

detecting whether the input includes a token;

if the token is detected in the input, checking what mode the processor is in;

if the processor is in a first mode, processing the input to render an arithmetic result;

if the processor is in a second mode, performing a token specific operation; and

producing an output.

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11. The method of Claim 10 wherein the input is comprised of at least one operand and at least operator; wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token; and wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode.

12. The method of Claim 10 wherein processing comprises executing at least one operation on the at least one operand according to the at least one operator to achieve a result.

13. The method of Claim 10 wherein performing comprises propagating the token; and wherein producing output comprises setting the output to be the token.

14. The method of Claim 10 wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request.

15. The method of Claim 10 wherein checking comprises checking a mode identifier.

16. The method of Claim 10 wherein checking comprises checking a mode identifier bit in a processor status register.

17. The method of Claim 11 wherein the first mode is a 32 bit word ISA mode and the second mode is a 64 bit word ISA mode.

18. A multi-mode processor comprising:

a plurality of instruction set engines;

a mode identifier;

a plurality of floating-point registers shared by the instruction set engines; and

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a plurality of floating-point units coupled to the floating-point registers, the floating-point units processing an input responsive to the mode identifier.

19. A method in a multi-mode processor comprising:

fetching an input from at least one of a plurality of floating-point registers;

detecting whether the input includes at least one token of a plurality of tokens;

if at least one token is detected in the input, checking what mode the processor is in;

processing the input to render an arithmetic result when the processor is in at least a first mode of a plurality of modes; and

performing a token specific operation when the processor is in at least a second mode of a plurality of modes.